

Lesson Plan

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	Discipline: ETC	Semester-4th Summer-2026	Name of the Teaching Faculty: Sri.Rabindra kumar satapathy(Guest Faculty ETC Engg.)
Sl. No.	Subject-Th.4.(ETCPE202) (VLSI Design)	No. Of Days/Week class alloted:03	Semester From date:-22.12.2025 To date: 18.04.2026 (No of weeks: 15)
	Weeks/Months	Class Day	Topic
1	4Th week 22nd dec To 31th dec	1st	Introduction to VLSI 1.1 CMOS Logic 1.2 Combinational and sequential circuits
		2nd	1.3 CMOS fabrication and layouts 1.4 Layout representations
		3rd	1.5 Stick diagrams 1.6 Design partitioning
2	1st week 1st jan To 09th jan	1st	1.7 Logic design 1.8 Circuit design
		2nd	1.9 Physical design
		3rd	1.11 Design Flow. 1.12 Modelling of MOS transistor
3	2nd week 12th jan To 17th jan	1st	1.13 Capacitance voltage characteristics 1.14 Non-ideal effects DC transfer characteristics
		2nd	1.15 MOS Inverter 1.16 MOS Transistor Switches
		3rd	1.17 CMOS Logic design 1.18 Circuit and System Representations
4	3rd week 19th jan To 22th jan	1st	1.19 Design Equations,
		2nd	1.21 Transistor Sizing 1.22 Static and Switching Characteristics
		3rd	1.23 Body Effect 1.24 Noise Margin
5	4th week 27th jan To 31th jan	1st	Delay and Power 2.1 Transient Response
		2nd	2.2 RC Delay Model 2.3 Effective Resistance
		3rd	2.4 Gate and Diffusion Capacitance 2.5 Equivalent RC Circuits
6	1st week 2nd feb To 07th feb	1st	2.6 Transient Response 2.7 Elmore Delay
		2nd	2.8 Layout Dependence of Capacitance 2.9 Determining Effective Resistance
		3rd	2.10 Linear Delay Model Logical Effort 2.11 Parasitic Delay
7	2nd week 9th feb To 13th feb	1st	2.12 Delay in a Logic Gate Drive 2.13 Extracting Logical Effort from Datasheets
		2nd	2.14 Limitationsto the Linear Delay Model 2.15 Logical Effort of Paths
		3rd	2.16 Delay in Multistage Logic Networks 2.17 Choosing the Best Number of Stages
8	3rd week 16th feb To 21th feb	1st	2.18 Sources of power dissipation 2.19 Dynamic power
		2nd	2.20 Static power 2.21 Wire Geometry
		3rd	2.22 Example of Metal Stacks 2.23 Interconnect Modelling, Resistance, Capacitance and Inductance
9	4th week 23th feb To 27th feb	1st	Circuit Design 3.1 Circuit Families
		2nd	3.2 Static CMOS 3.3 Ratioed Circuits
		3rd	3.4 Cascode Voltage Switch Logic

10	1st week 2nd march To 07th march	3rd	3.4 Cascode Voltage Switch Logic 3.5 Dynamic Circuits
		1st	3.6 Pass-Transistor Circuits 3.7 Sequencing Static Circuits
		2nd	3.8 Sequencing Methods 3.9 Max-Delay Constraints
11	2nd week 9th march To 13th march	3rd	3.10 Min-Delay Constraints 3.11 Time Borrowing
		1st	3.12 Clock Skew 3.13 Circuit Design of Latches and Flip-Flops
		2nd	3.14 Conventional CMOS Latches 3.15 Conventional CMOS Flip-Flops
12	3rd week 16th march To 20th march	3rd	3.16 Pulsed Latches 3.17 Resettable Latches and Flip-Flops
		1st	3.18 Enabled Latches and Flip-Flops
		2nd	3.19 Incorporating Logic into Latches
13	4th week 23th march To 31st march	3rd	IV Subsystems Design 4.1 Adders, zero one detectors
		1st	4.1 Adders, zero one detectors
		2nd	4.2 Comparators, counters
14	1st week 2nd april To 10th april	3rd	4.3 Memory subsystems SRAM
		1st	4.4 Read and write operation
		2nd	4.5 DRAM
15	2nd week 13th april To 18th april	3rd	4.3 Memory subsystems SRAM
		1st	4.4 Read and write operation
		2nd	4.5 DRAM
		3rd	4.6 Sense amplifiers

[Signature]
Signature of the Teacher

22/12/2025